Chapter 4

Development of CSA doped PANi-Ta_2O_5 based organic field effect transistors for NO_2 gas sensing

4.1 Introduction: Organic Field Effect Transistors

Organic field effect transistors (OFETs) were discovered in 1987 [200] and emerged as a potential building block of electronic devices since the pioneering work on OFETs by Kudo et al. [201] and Koezuka et al. [202].

Kudo et al. [201] reported in 1984 on mobility measurement of merocyanine, an organic semiconductor material using the field effect concept. After this first report, Koezuka et al. described the first OFET based on polythiophene in 1987. They investigated the device parameters of the OFET and established the device as highly stable.

Since then extensive research on OFETs has begun. The carrier mobility of the OFETs reached the same level as the poly silicon FETs in the late 1990s. Y. Yuan et al. [203] achieved hole mobility of 43 cm^2/V-s of OFETs based on meta stable blended solution of 2,7-dioctyl[1]benzothieno[3,2-b][1]benzothiophene (C8-BTBT) and polystyrene, the highest value reported till date of all organic semiconductors.

J. Takeya et al. [204] reported contact-free intrinsic mobility of 40 cm^2/V-s of a single crystalline rubrene based OFET. L. Xiang and co workers achieved the highest electron mobility of 13 cm^2/V-s of an n-channel OFET based on Fullerene (C60).

Most of the practical applications today are dominated by p-type OFETs owing to their ease of synthesis and fabrication process, relatively high value of carrier mobility etc. Many of the high performance OFETs based on conjugated polymers are p-types, some of which show hole mobility more than 20 cm^2/V-s with good device stability. On the other hand, development of ambipolar [205], [206], [207] or n-type semiconductors [208], [209], [210] has been less progressed due to their relatively low electron mobility and inferior device stability [211]. Practical transistors require high mobility, large current on/off ratio, high stability and low threshold voltage. Many researchers have successfully implemented p-type OFETs to achieve these merits [212], [213].

OFETs have now been considered as a key component in modern microelectronics design. In contrast to their inorganic counterparts, OFETs have shown attractive properties such as flexibility, low cost, tailor-made molecular design, room temperature operation, easy compatibility with large area and flexible substrates, which endow them as a favorable candidate for numerous applications such as light-emitting field-effect transistors, active matrix flat panel displays, radio frequency identification transponders, smart cards etc.

In the field of gas sensing, OFETs have gained massive attention over the past several decades. OFETs can be functionalized sophisticatedly with regard to their excellent response to a variety of external stimuli. This is promoted by the inherent advantages of OFETs such as low cost, mechanical flexibility, tunable molecular structure, solution processibility, large-scale production and ability for multi-parameter accessibility. This has provided OFETs enormous potential as reliable gas sensors with high sensitivity and selectivity, and good stability.

Tremendous efforts have been devoted to synthesize novel, high quality organic semiconductors (OSCs) for using them in OFET based gas sensors. Initiation of innovative fabrication protocols, study of suitable gate dielectrics, interface engineering have been the areas of research to produce high performance OFETs. OFETs are easily susceptible to chemical interactions and photo excitation and easily undergo structural changes. These factors make them desirable for detecting physical and chemical targets. Their effective response towards light, pressure, chemicals have made them indispensable component in interdisciplinary fields of organic electronics, material science, bioscience and sensor electronics [214].

Another important flagship of OFETs is the ability of multi-parameter response such as charge carrier mobility, threshold voltage, current on/off ration and bulk conductivity of the OSC film. This is also the reason that OFETs can detect more than one analyte at a time. Such devices can provide fingerprint response towards a large variety of analyte gases at a low concentration [215]. These factors have made OFETs a strong contender among the commonly used two-terminal chemiresistors. Thin film based chemiresistive NO_2 gas sensor has been implemented and discussed in chapter 3. Chemiresistors exhibit change in resistance when exposed to an analyte gas, but in many cases they have not delivered satisfactory

results. In the present chapter, the implementation and study of OFET based NO_2 gas sensor are presented.

Although MOSFETs have been popular research tool in the semiconductor field, OFETs have attracted enormous attention since the last decade due to their inherent advantages of light weight, large area coverage, low processing cost, structural flexibility and room temperature processing. Great efforts have been devoted to achieve improved carrier mobility (for high on current and high speed) in order to implement OFETs in practical applications such as sensor arrays, flexible organic electronics, organic CMOS circuits for radio frequency identifications (RFIDs), pixel driving for organic light-emitting diodes (OLEDs) etc.

4.1.1 Structure of OFETs

Though OFETs look similar to a conventional MOSFET, the basic difference lies in the fact that there is no diffused n-type region at the source and drain electrodes. The small drain current at zero gate voltage results due to very weak conductivity of the organic semiconductor. Fig. 4.1 shows the schematics of p-MOSFET and OFET.

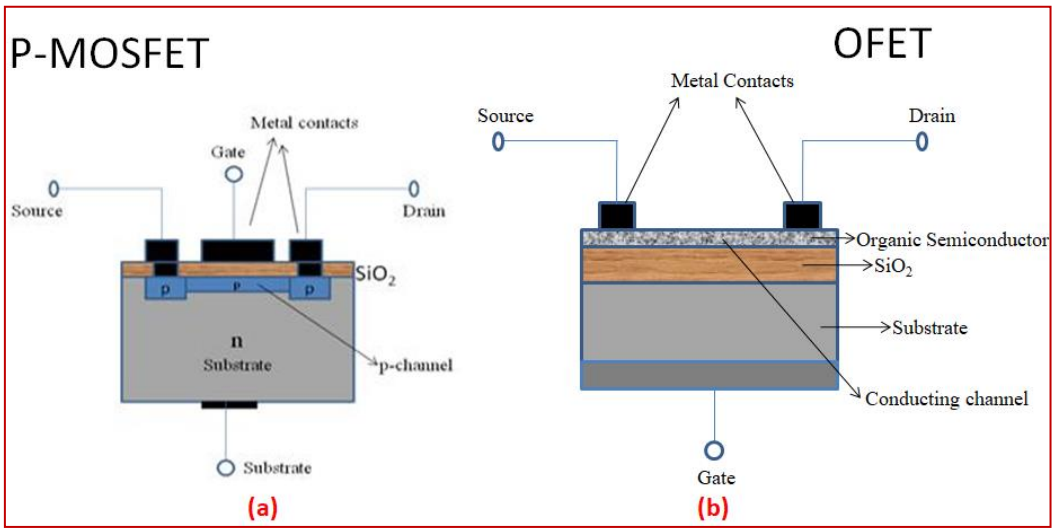

Fig. 4.1. Schematic diagram of a) p-channel depletion type MOSFET [217], b) OFET.

The conducting channel in OFET does not correspond to the formation of an inversion layer like in MOSFET but rather to an accumulation layer at the semiconductor/insulator interface. In practice, the drain current voltage plots depict a linear behavior at low drain voltage, and then saturates as the drain voltage approaches gate voltage [216].

From the points of view of structure and operation, OFETs could be considered as two-terminal organic chemiresistors when no gate voltage is applied. In contrast to the two-electrode organic chemiresistors, one of the most discerning advantages of the use of OFETs is their intrinsic capability to modulate the electric performances with a gate voltage. This makes OFETs as multi-parameter electronic device, where a number of key parameters, such as charge carrier mobility, threshold voltage, saturation current, current on/off ratio, sub threshold swing could be extracted separately and easily [214]. Together with the considerable variety of the OSCs, OFETs have emerged as a promising platform for a huge range of applications such as chemical and bio sensors, memory [218], [219], complementary integrated circuits [220], flexible displays [221].

Organic transistors are constructed using thin film architecture as shown in Fig. 4.2. A field effect transistor is essentially a capacitor where one of the plates is represented by a semiconducting layer (in case of OFETs). The other plate is the gate electrode. The insulating layer between the semiconducting layer and the gate electrode is called the gate dielectric. The semiconducting film is equipped with the source and the drain electrodes, separated by a distance, called channel length, L, wherein the conducting channel of the device lies. The width of the source and the drain electrodes is called the channel width, W. The gate electrode can be a metal or an organic polymer. As gate dielectrics, inorganic insulators such as SiO_2, polymeric insulators such as poly(methyl methacrylate) (PMMA) or poly(4-vinylphenol) (PVP) or high-k dielectrics (Al_2O_3, TiO_2, Ta_2O_5, HfO_2) are used. For the source and drain electrodes which inject charge into the semiconductor layer, high work function metals such as gold, aluminum, platinum or printable polymers such as PEDOT:PSS, PANi are used [222]. Fig. 4.2 shows the structure of field effect transistor with a top view.

When a voltage is applied between the source and the gate (V_{GS}), an equal amount of charge of opposite sign is generated at either side of the gate dielectric. The charge induced at the interface of the insulator and the semiconductor can be set in transit by applying a second voltage between the source and the drain (V_{DS}). This is the working principle of an organic field effect transistor which is also called as organic thin film transistor (OTFT). In practice, the OFET works as a variable resistance, whose magnitude is controlled by the gate voltage.

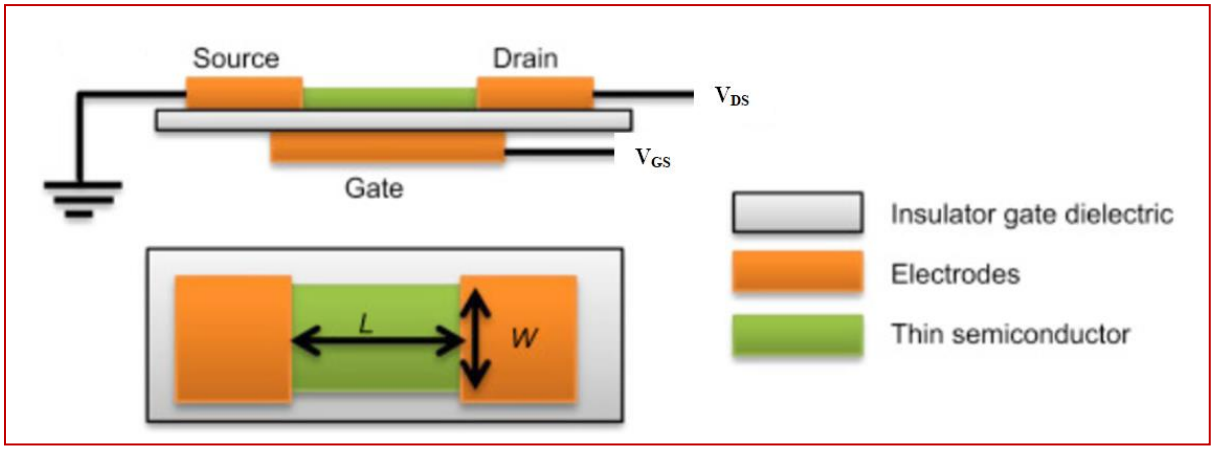

Fig. 4.2. Schematic of a field effect transistor [222].

A thin film transistor (TFT) is a field effect transistor (FET), similar to the metal-oxide field effect transistors (MOSFET) which is the most important constituent in the design and construction of modern integrated circuit technology. In case of an OFET, organic semiconductors like conducting polymers or their nanocomposites can form the active layer (conducting channel). Though TFT was patented in the late 1920s, no practical applications emerged and it faded away in the competition with MOSFET technology. In the early 1970, there was increasing demand for large area applications in flat panel displays and this has motivated the acceptance and blooming of TFT technology. Since the mid 1980s, TFTs became the frontrunner in the field of liquid crystal display and organic light emitting diodes. In the 1990s, organic semiconductor based TFTs have been developed with electron mobility comparable to that of hydrated amorphous silicon [223].

To achieve the optimum performance, the transistor must deliver the lowest off current and the highest possible on current. The magnitude of the latter is determined by the carrier mobility of the semiconductor. In single crystalline silicon, carrier mobility is in the order of 10^3 $cm^2/V\text{-}s$. Earlier OFETs offered lower range of mobility, typically in the range of 10^{-4} $cm^2/V\text{-}s$ or even lower. Much effort was then put forth to deal with the various challenges to improve the mobility. As the mobile charges are generated in the conducting channel located in the vicinity of the insulator-semiconductor interface, it is soon envisaged that purity, high ordering, grain size of the semiconductor material can play very significant roles [224]. These factors largely depend on the deposition techniques as discussed in the earlier chapter.

In case of polycrystalline organic layer, mobility mainly depends on the orientation and crystal grain size as reported by Dodabalapur et al. [225]. They worked on using low rate deposition and increased substrate temperature to achieve a higher mobility. Even higher mobility OFETs based on single crystal OSCs such as pentacene [226], [227], sexithiophene [228], rubrene [204] have been reported in the literature. This can outperform amorphous silicon based transistors. Horowitz et al. [229] developed a model that established that charge transport in OFETs is limited by carrier hopping between the grains. Also, the model predicted that carrier mobility should improve with the increase in grain size. Y. Takatera et al. [230] demonstrated that increase in grain size can lead to high carrier mobility for a top-gate n-type OFET utilizing perylene dimide derivate film.

In the literature, p-type OFETs (majority charge carriers are holes) have mostly been reported. N-type organic compounds are quite desirable as they could allow the design of circuits using a complementary architecture giving away numerous advantages. However, the performance of n-type semiconductors is less satisfactory than that of p-type semiconductors. Most n-type organic semiconductors are sensitive to oxygen, which requires the fabrication process to carry out under strict control of the ambient environment [231]. Also, the mobility of n-type OFETs is one order less than that of p-type OFETs [232], [233]. Efforts have been made to mitigate these shortcomings.

S.K. Park et al. [234] fabricated high performance n-type OFETs based 2-D terraced structure of the novel dicyanodistyrylbenzene (DCS) derivative using simple solution processing to acieve electron mobilities of 0.55 cm^2/V-s. L. Xiang et al. [235] demonstrated C60 based n-type OFETs by optimizing the interfacial of tetratetracontane (TTC) and different polymeric dielectrics (PVA/PMMA). They obtained an incredibly high electron mobility of 13.6 cm^2/V-s. S. Lan et al. [236] observed an improvement of device characteristics by blending an appropriate amount of a p-type organic semiconductor with the n-type semiconductor.

There can be four different architectures of OFETs as shown in Fig. 4.3, depending on which the transistor can show very different behavior. They are named according to the relation of the semiconductor layer and the gate dielectric as bottom contact top gate (BCTG), bottom contact bottom gate (BCBG), top contact bottom gate (TCBG) and top contact top gate (TCTG). The most common configuration is the ones with the semiconductor layer deposited on the top of the dielectric with the underlying gate electrode. The charge injecting source

and drain electrodes providing the contacts are defined either on top of the organic film (TCBG) or on the surface of the substrate prior to the deposition of the semiconductor layer (BCBG).

In the bottom contact OFET structure, electrodes are formed on the gate dielectric and then the semiconductor layer is deposited. Microfabrication technologies can be applied to form the electrodes and hence small channel length is achievable. But there can be discontinuity between the electrodes and the semiconductor layer, giving rise to high contact resistance and low carrier mobility. In case of top contact structure, the electrodes are made as the last step above the organic semiconductor layer. So microfabrication techniques are difficult to apply and as such, small channel length is not feasible. However, top contact design results in low contact resistance and high carrier mobility [237].

Fadilondi et al. [237] fabricated both top contact and bottom contact OFETs, and obtained carrier mobilities of 0.2 cm^2/V-s and 0.02 cm^2/V-s for the two configurations respectively. K. Kim and co-workers [238] demonstrated single crystal rubrene based top-contact, p-type OFETs with spin coated poly (4-hydroxystyrene) as the gate dielectric and achieved carrier mobility of 1.12 cm^2/V-s, V_{TH} of -0.3 V, current on/off ratio of 10^2 and 1.6 nA of leakage current. They established that the device exhibited improved performance over the OFET devised with ceramic dielectric silicon nitride (Si_3N_4) in bottom contact configuration.

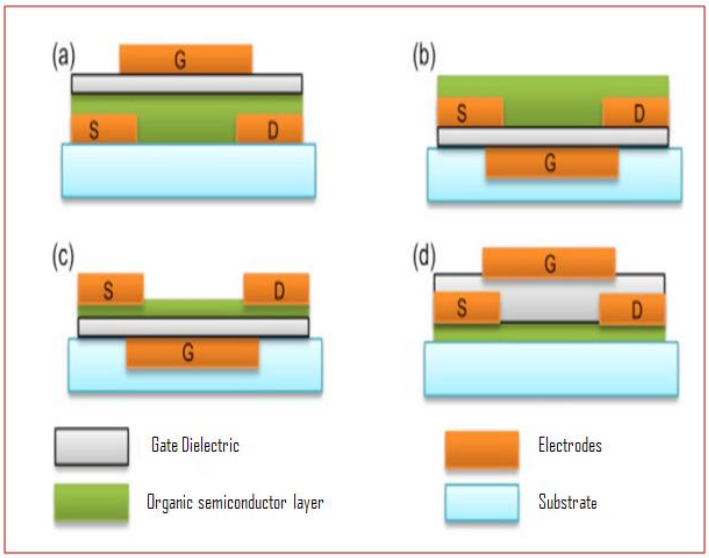

Fig. 4.3. Schematic representation of different architectures of OFETs –a) BCTG, b) TCBG, c) TCBG, d) TCTG [222].

4.1.2 OFETs in NO_2 gas sensing

High performance OFET based gas sensors have been extensively researched since the last few decades. Gas sensors based on OFETs are found more suitable for practical applications than their inorganic counterparts which usually operate at high temperature. Gas analytes react with the active layer of the OFET as follows – i) the analyte molecules get adsorbed on the active layer surface, ii) the adsorbed molecules penetrates into the active layer, iii) the analyte molecules undergo various interactions such as van der waals force, dipole-dipole interactions, hydrogen bonding etc. [239]

Keeping in view the aggravated scenario of the world ecosystem caused by the continual adverse effects of various pollutant gases, there has been an extreme demand for a highly effective system to detect these hazardous gases. NO_2, being a major air pollutant, has been a serious threat to the environment and the living beings. This issue is discussed in chapter 1.

NO_2 is an electron withdrawing gas, which typically shows opposite effects to OFET devices compared to the reducing gases like NH_3. It normally increases the drain current in p-type OFETs and decreases the drain current in case of n-type OFETs. But at very high concentration, more complicated mechanisms may involve such as the deterioration of the active layer, oxidation of the semiconductor layer [240].

4.1.2.1 Use of hybrid materials in OFETs for NO_2 gas sensing

In recent years, extensive research efforts have been employed to gas sensors to diagnose the presence of NO_2 gas in the environment at a lower concentration level. OFET based NO_2 gas sensors have shown tremendous potential in delivering the desired outputs with high response and selectivity, better stability, low temperature operability and reduced cost [239], [241], [242], [243].

Lot of efforts have been invested to develop novel organic semiconductors comprising of conducting polymers, small molecules and hybrid materials comprising of inorganic compounds. The overwhelming surge of very innovative means of functionalizing the sensing layer for effective gas detection and device optimization has been witnessed in many of the past reports.

M. Mirza et al. [244] employed ultrathin monolayer of pentacene for the design of their OFET and achieved enhanced sensing response and selectivity towards sub ppm level of NO_2 with an increase in carrier mobility and shift in threshold voltage. Z.Yang and co-workers [46] worked on developing a bulk polymer hetero junction comprising of semiconducting poly(3-hexylthiophene-2,5-diyl) (P3HT) and insulating poly(9-vinylcarbazole) (PVK) to study NO_2 sensing performance. They obtained the current sensitivity of approx. 12381% for 15 ppm NO_2 with 50% P3HT, which is 30 times improved than that of pure P3HT. S. Han et al. [246] utilized ZnO/PMMA hybrid dielectric and CuPc/Pentacene heterojunction to devise high-performance OFET for NO_2 detection. H. Fan et al. [247] reported OFET device based on heterojunction consisting of p-type copper phthalocyanine (CuPc) and n-type dioctyl perylene tetracarboxylic diimide (PTCDI-C8) with one order of enhanced sensitivity towards NO_2 gas compared to the device with single layer of CuPC. S. Han et al. [242] demonstrated OFET based NO_2 gas sensor utilizing hole transporting poly(3-hexylthiophene-2,5-diyl) (P3HT) and electron blocking poly(9-vinylcarbazole) (PVK) in 1:1 blend and achieved sensor response 40 times more than that of pure P3HT.

A revolutionary approach in gas sensing has been to utilize hybrid materials, viz., materials that are comprised of two or more constituents with different properties. As demonstrated by the several past researchers cited above, gas sensors employing hybrid materials could possess enhanced gas sensing results compared to that of using single component. Gas sensors like the OFETs utilizing single material with intrinsic sensing activity may be inhibited by several hindrances at different levels such as – lack of long-term stability and sensitivity due to high affinity of the CPs towards the VOCs and humidity present in the atmosphere, low carrier mobility, high operating voltage etc. These issues can be minimized by functionalizing the host polymer with another organic or inorganic constituent at nanostructure or molecular level. The resultant properties of the hybrid material which are largely determined by the interfacial characteristics can thus be achived through material engineering to meet the desired outcome.

There are bountiful hybrid materials in complex constituents and new kinds of nanostructures, which pave the path of utilizing these materials as gas sensitive transducers exploiting unheard-of numerous sensing behaviours. With hybrid materials, more enhanced mechanisms involving chemical and physical processes can happen through catalytic reactions with analytes, charge carrier transport, molecular binding and maneuvering

hetrojunctions. This enables precise designing, controlling and enhancing sensing performance [248].

Among the CPs, PANi is one of the most commonly used material in gas sensing applications due to its simple chemical structure, good environmental stability, easy synthesis process, interesting redox property, and relatively high conductivity [17]. It has been discussed earlier that PANi has been functionalized successfully with nanoparticles of metal oxides and acid doping in order to achieve interesting results in the field of gas sensing [30], [32], [61], [248]. The advantages of pristine PANi, PANi nanocomposite involving inorganic metal oxides and doping effects of organic/inorganic acids towards gas sensing are discussed in detail in chapter 2.

4.1.2.2 Choice of selection of gate dielectric

Besides the considerable research taking place for the OSCs, research and development of the gate dielectrics have equally attracted substantial importance in the recent days to achieve high performance OFETs. OFETs based on pentacene, rubrene and many other CPs have been showing high carrier mobility, but their operating voltage found to be high. To achieve low operating voltage, the drain current needs to be high. This can be obtained using high capacitance gate dielectric [249]. The capacitance (per unit area) for a dielectric layer is given by the following equation.

$$C = \frac{\varepsilon_o . \varepsilon_r}{t} \qquad (4.1)$$

Where ε_o is the permittivity of vacuum, ε_r is the dielectric constant (k) and t is the dielectric layer thickness. Thus, the capacitance can be increased by increasing the dielectric constant and/or reducing the thickness of the dielectric layer. Also, the drain current is proportional to the dielectric constant and the gate voltage as evident from the following drain current equation of the OFET.

$$I_{DS} = \frac{W}{L} \mu C_i \frac{1}{2} (V_{GS} - V_{TH})^2 \qquad (4.2)$$

Where μ is the field effect carrier mobility, I_{DS} is the drain current, V_{GS} is the gate voltage, V_{TH} is the threshold voltage, W and L are the channel width and length respectively, and C_i is the capacitance of the gate dielectric per unit area.

Therefore, it is suggested to use high-k dielectric material for the gate to accumulate the necessary charge in the conducting channel at a low operating voltage [250]. There have been reports of using high-k metal oxide dielectrics such as Al_2O_3 (aliminium oxide, k=9) [251], HfO_2 (hafnium oxide, k=25) [252], Ta_2O_5 (tantalum oxide, k=22) [253], barium zirconate titanate [254] in place of conventional SiO_2 to ensure low operating voltage and hence reduced power consumption. It is found that these less known oxides have inferior electronic properties compared to SiO_2 such as their tendency to crystallize and high density of electronic defects [255]. Moreover, these inorganic metal oxides have high thermal properties, often give rough surface and are difficult to cast on a large surface. As reported by many groups, the use of high-k dielectric can result in a declining mobility caused by high dipolar disorder at the semiconductor/dielectric interface due to carrier localization and surface polarization of the high-k material leading to degrading of device performance [256], [257].

On the other hand, though the polymeric dielectrics have comparatively smaller value of k, they can be solution processed and are compatible with flexible substrates. They also have non-interfering nature due to the organic-organic interface [258] and can offer highly smooth surface helping in the proper growth of the semiconductor layer [259]. A polymeric dielectric can operate at a low processing temperature, can reduce the leakage current [260] and facilitate a trap-free semiconductor/dielectric interface enhancing the charge carrier mobility [257]. It was also reported that incorporating low-k gate dielectric in OFETs, one could expect better current modulation, low hysteresis and low threshold voltage [261]. Low-k dielectrics also have the advantages of being less vulnerable to ionic impurities, which can flow under with the application of gate voltage and render device instability [262].

However due to low dielectric constant, the polymer dielectrics have low capacitance leading to high operating voltage and high threshold voltage. These issues can be overcome by unifying the advantages of high-k oxides for low voltage and low-k polymer for high quality surface with meticulous blending of the two [252], [258], [259], [263].

PMMA is a synthetic resist synthesized from the polymerization of methyl methacrylate used in high resolution process of nanolithography that uses electron beam, UV or X-ray radiation. It possesses good thermal and mechanical stability, and a high resistivity greater than 10^{15} ohm-cm. PMMA has a permittivity of 2.6 at 1 MHz and a dielectric constant of 3.9 at 60 Hz [264]. These properties make PMMA similar to silicon di-oxide and hence it becomes suitable to be used as dielectric. Also, it is easier to deposit PMMA using spin-coating method and baked at low temperature [265]. PMMA has been functionalised with other materials and used as novel gate dielectric in the design of OFETs by several past works to achieve promising results.

L. Shang et al. [258] devised a low voltage CuPc based OFET utilizing PMMA and ZrO_2 (zirconium oxide) bilayer. The dielectric leakage current reduced to one order of magnitude compared to that on using with ZrO_2 single layer. The rightful combination of PMMA and ZrO_2 provided a smooth semiconductor layer and an improved interface with low threshold voltage and zero hysteresis. Deman et al. [266] demonstrated pentacene OFETs using Ta_2O_5 and PMMA bilayer as the gate dielectric. When used with only Ta_2O_5, the device exhibited very low operating voltage attributed to high k of Ta_2O_5, but with some surface trapping and gate leakage current. By incorporating PMMA layer on Ta_2O_5, an improved interface with pentacene was achieved with considerable decline in gate leakage current. Jung et al. [267] reported an n-type OFET utilizing cross-linked PMMA and attained a small threshold voltage of 0.1 V and operating voltage less than 3 V. X. Li et al. [268] utilized PMMA and silk fibroin bilayer dielectric in the design of the OFETs and obtained superior NO_2 gas sensing performance.

The chemiresistive thin film sensor utilizing CSA doped PANi-Ta_2O_5 is studied in the present work. The sensor exhibited good gas sensing properties towards NO_2 as detailed in chapter 3. The OFET based NO_2 sensor device utilizing the same material is designed in the subsequent work. The experimental details and results of the sensor device are discussed in sections of 4.3 and 4.4.

4.2 Basic operation of an OFET

Fig. 4.4 illustrates different operation regimes of field effect transistor. Here, source, drain and gate contacts are denoted by S, D and G. The gate electrode is applied with a voltage V_{GS}

and the drain electrode with a voltage V_{DS}. Normally, the source electrode is connected to ground. There are two operating regimes – linear and saturation. The transistor conducting channel is formed at the interface of the OSC and the gate dielectric. Holes are accumulated when a negative V_{GS} is applied which leads to p-type conduction. When a positive V_{GS} is applied, n-type conduction is obtained. Ambipolar conduction is achieved when the device operates in both the voltage regimes [222]. The type conduction depends on the intrinsic property of the OSC and the choice of the contact material [269]. Since the present work involves development and study of p-type OFET, p-type operation is discussed in the following sections.

Minimal current (I_{off}) exists between S and D electrodes when no gate voltage ($V_{GS}=0$) is applied. At this time, the device is in "off" state. When a gate voltage, V_{GS} is applied, charges will be induced and confined at the insulator/semiconductor interface (Fig. 4.4.a). At this point, the device comes under accumulation mode. The number of charges induced is proportional to V_{GS} and the capacitance C_i of the insulator. With a small voltage V_{DS} imposed at the drain, accumulated charges start moving between source and drain, creating a current, I_{DS}. The device now is in the "on" state ($V_{GS}<0$). Fig. 4.4.b shows the field effect transistor working under linear regime. However, not all the induced charges will be in transit and contribute to the current in the device. Some of the induced charges will fill in the deep traps first before the additionally induced charges participate in the movement.

When the traps are filled, the gate voltage is called the threshold voltage, V_{TH}. Hence, on order to accumulate carriers, the gate voltage is to be applied higher than the threshold voltage ($V_{GS} > V_{TH}$). The channel reaches "pinch-off", when V_{DS} is further increased and V_{DS} equals to V_{GS}-V_{TH} (Fig. 4.4.c). A depletion region forms adjacent to the drain because of the difference in the local potential V(x) and the gate voltage comes below the threshold voltage, V_{TH}. The space-charge-limited saturation current $I_{DS,sat}$ flows across the narrow depletion area. From this point, the field effect transistor works in the saturation regime. Even if V_{DS} is increased further, the current will not substantially increase because the potential at pinch-off point remains at V_{GS}-V_{TH} and hence the potential drop between that point and the source electrode kept almost same, and the current saturates at a value of $I_{DS,sat}$ (Fig. 4.4.d) [222].

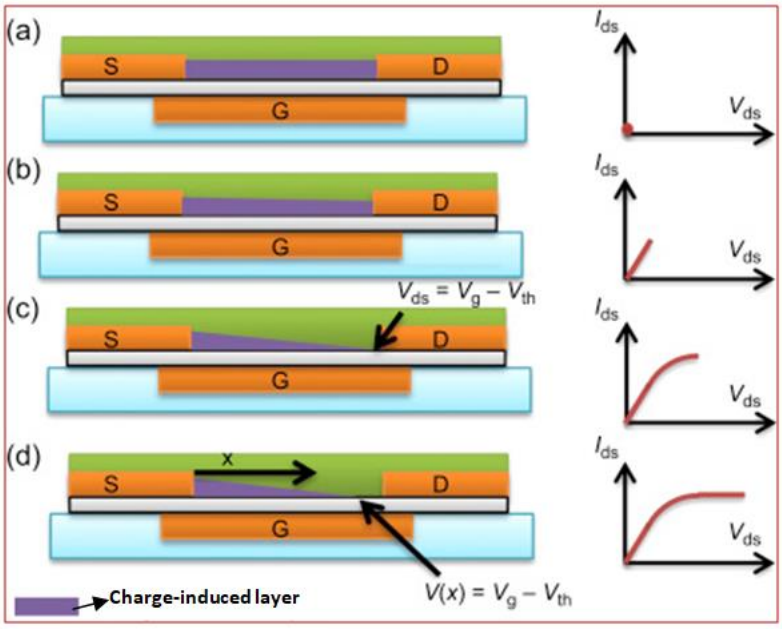

Fig. 4.4. Different operation regimes of field effect transistors: a) generation of charges induced, b) linear regime, c) start of saturation regime at pinch-off, and d) saturation regime [222].

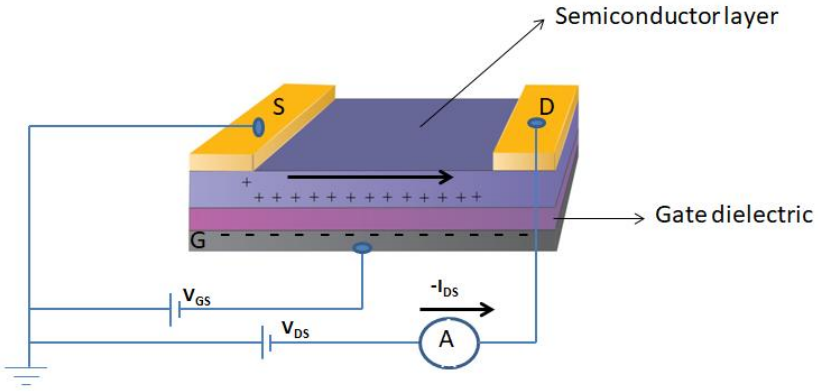

Fig. 4.5. Operating mechanism of p-type OFET (both V_{DS} and V_{GS} are negative) [263].

Fig. 4.5 shows the operation of a p-type OFET, where both drain voltage and gate voltage are negative. OFETs usually operate in the accumulation mode, where the bias applied at the gate induces charge at the semiconductor/insulator interface. The gate bias is applied negative in case of most p-type OFETs. This negative gate voltage ($-V_{GS}$) caused the accumulation of positive charge carriers at the semiconductor/insulator interface which subsequently participated in the current flow ($-I_{DS}$) with the application of the drain voltage ($-V_{DS}$). Once the gate voltage is positive, it leads to the formation of depletion layer and subsequent

decrease in drain current (I_{DS}). The positive gate voltage for p-type OSCs invokes the depletion mode of the device, wherein the carriers are pushed back from the semiconductor interface leading to a decrease in drain current. The gate voltage (V_{GS}) controls the accumulation of carriers in the semiconductor/dielectric interface, while the drain voltage (V_{DS}) drives the current I_{DS} between source and drain [17], [270].

This scenario is illustrated in the energy band structure of the metal contacts, dielectric and the OSC of the p-type OFET in Fig.4.6.

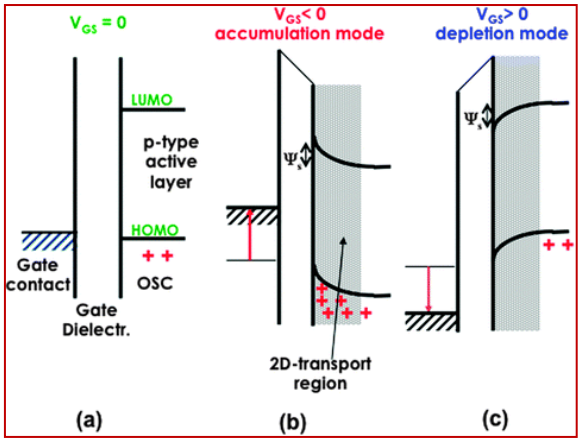

Fig. 4.6. Energy band diagram of gate contact, insulator and the OSC of the OFET [270].

There exists a small collection of positive charges at the p-type semiconductor layer at V_{GS}=0 (Fig. 4.6.a). When a negative gate voltage (V_{GS}<0) is applied (Fig.4.4.b), positive charges are induced and accumulated at the semiconductor/dielectric interface forming a conducting channel between the source and drain contacts. The charge transport at V_{GS}=0 is three dimensional as it involves the charge in the entire bulk of the OSC. The field generated by a negative V_{DS} causes the charges in the conducting channel to move in a direction perpendicular to the drawing plane. The more is the magnitude of the negative gate voltage, the more is the accumulated charge density and hence a greater value of the drain on current (I_{ON}). This is the accumulation mode operation of the device as shown in Fig.4.4.b. For a positive gate voltage (V_{GS}>0), the HOMO and LUMO levels of the p-type OSC tend to bend upwards and this causes the charges move towards the bulk of the OSC (Fig.4.4.c). This results in the constriction of the conducting channel reducing the drain current and the device undergoes depletion mode [270].

As V_{GS} is applied, accumulation of charge is set, but I_{DS} on current does not flow until the gate voltage reaches a value called the threshold voltage (V_{TH}). This is the gate voltage required to turn the device "ON". In a thin film transistor, V_{TH} is in fact equal to Q_{trap}/C_i, where Q_{trap} is the density of charge once injected in the channel, migrated into the deep traps and C_i is the dielectric capacitance per unit area. Deep traps are low mobility states (far from the delocalized states) that are possibly originated by the impurities and/or structural defects located in the crystal grain or grain boundaries of the OSC. So, V_{TH} is the gate bias required to induce the charge, Q_{trap}, to completely fill in the deep trap levels. Once all traps are filled, the further injected charges can move along the delocalized molecular orbital with a given mobility, through the channel under the applied V_{DS} bias [270].

The typical current-voltage characteristics for the linear and saturation regimes are shown in Fig.4.7. The transfer characteristics (Fig. 4.7.a, 4.7.b) show that at first I_{DS} increases linearly with V_{GS} when the gate voltage exceeds V_{TH}. In the saturation regime, the square root of the saturation current is directly proportional to the gate voltage. The carrier mobility depends on the ratio of I_{DS} and $(V_{GS}-V_{TH})^2$. The source-drain current I_{DS}, with the increase of source-drain voltage V_{DS} at different gate voltages comprising of both the regimes gives the output characteristics of the device (Fig. 4.7.c) [23], [271].

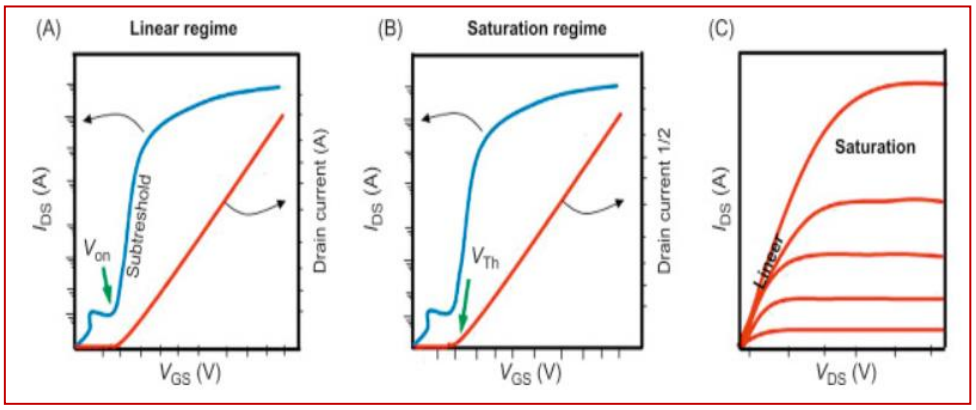

Fig. 4.7. Representative current-voltage characteristics of an OFET: a), b) transfer characteristics in linear and saturation regime, c) output characteristics showing both the linear and saturation regime [271]

The output curves (I_{DS} vs V_{DS}) are plotted in a linear region at $V_{DS} << (V_{GS}-V_{TH})$ and in a saturation region at $V_{DS} > (V_{GS}-V_{TH})$. Fig. 4.8 shows the two regimes of the output characteristics. At lower values of V_{DS}, I_{DS} increases linearly with V_{DS} following Ohm's law

at a fixed V_{GS} (linear regime - Fig.4.8.a). As V_{DS} becomes more negative, positive charges accumulated get depleted near the drain contact region. At this point, the field generated by V_{DS} overpowers the gate voltage and the conducting channel becomes narrow at the drain contact, called "pinch-off". Here, the two dimensional confinement of the charges is lost and I_{DS} reaches a constant value called the saturation current, $I_{DS,SAT}$ (saturation regime– Fig.4.8.b and 4.8.c).

At low V_{DS}, the drain current (I_{DS}) increases linearly with the applied drain voltage at a fixed V_{GS} according to the following equation.

$$I_{DS,lin} = \frac{W}{L}\,\mu\, C_i\,(V_{GS} - V_{TH})V_{DS} \quad , V_{DS} \ll (V_{GS} - V_{TH}) \quad \text{----- linear regime} \qquad (4.3)$$

At large V_{DS} ($V_{DS} > V_{GS}$-V_{TH}), the drain current reaches a value and the device enters saturation regime. The saturated drain current follows equation 4.4.

$$I_{DS,SAT} = \frac{W}{L}\mu C_i \frac{1}{2}(V_{GS} - V_{TH})^2 \quad , V_{DS} > (V_{GS}\text{-}V_{TH}) \quad \text{---- saturation regime} \qquad (4.4)$$

$$\mu_{sat} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2 \qquad (4.5)$$

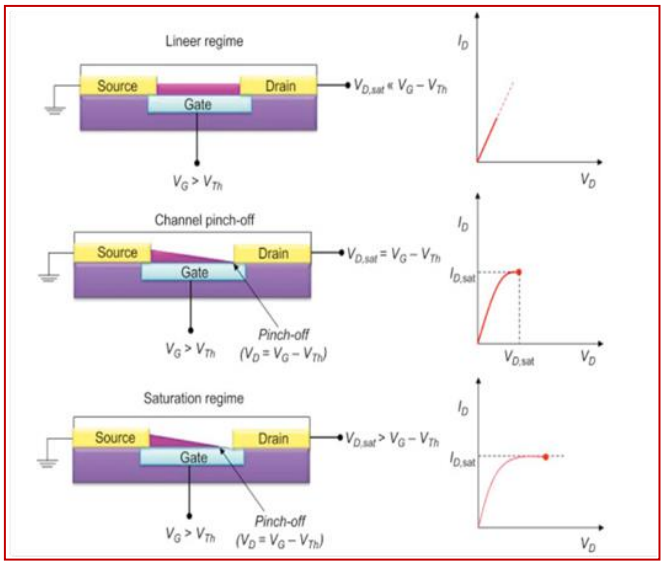

Fig. 4.8. Working conditions of OFET and its output characteristics: a) linear regime, b) onset of

saturation regime at pinch-off, c) saturation regime (V_G-gate voltage, V_D-drain voltage, I_D-drain current, V_{Th}-threshold voltage) [270].

Fig. 4.8.b shows the square root of $I_{DS,SAT}$ versus V_{GS} transfer curve at constant V_{DS} taken at saturation region. The value of carrier mobility, μ (saturation region) can be extracted graphically from $\sqrt{I_{DS}}$ versus V_{GS} plot by solving equation 4.4 and can be calculated using equation 4.5. The threshold voltage, V_{TH} can be obtained by extrapolating the transfer curve.

4.3 Experimental

4.3.1 Material preparation

The synthesis process and preparation of PANi-Ta_2O_5(50wt%) doped with CSA(40wt%) is described chapter 2. This nanocomposite is used as the sensing layer of the OFET device.

4.3.2 Material characterization

The PANi-Ta_2O_5-CSA40% was characterized by SEM, TEM, FTIR, UV-Vis and XRD methods. The findings are elaborated in chapter 2.

4.3.3 Fabrication of the OFETs based on PANi-Ta_2O_5-CSA40%

ITO (indium tin oxide) coated glass substrate (0.5 cm × 0.5 cm) was cleaned thoroughly using RCA1 followed by RCA2 and then dried at room temperature. The OFET device was constructed on ITO coated glass substrate which also served as the bottom gate electrode.

PMMA was prepared by performing free radical polymerization of methyl methacrylate and benzoyle peroxide as the initiator at room temperature. 10 mg of PMMA was diluted in 100 ml of anisole (Merck) and was used as the dielectric layer. PMMA solution was spun onto the ITO coated glass substrate using spin coating method at 800 rpm for 80 seconds (Fig. 4.9-spin NXG-M1). The PMMA layer was then dried in a conventional oven at 50^0C for 1 hour. The thickness of the PMMA layer was measured 900 nm as determined by Spectroscopic Ellipsometer (Make: Semilab).

Fig. 4.10 shows the Plasma-Enhanced Chemical Vapor Depostion (PECVD) system used to deposite silicon-dioxide (SiO_2) layer for the test glass substrate-SiO_2 based OFET.

Fig. 4.9. Photograph of the spin coating machine used (spin NXG-M1) [courtesy-microfabrication lab facility, Tezpur University].

Fig. 4.10. Photograph of the plasma-enhanced chemical vapor deposition (PECVD) system [courtesy-microfabrication lab facility, Tezpur University].

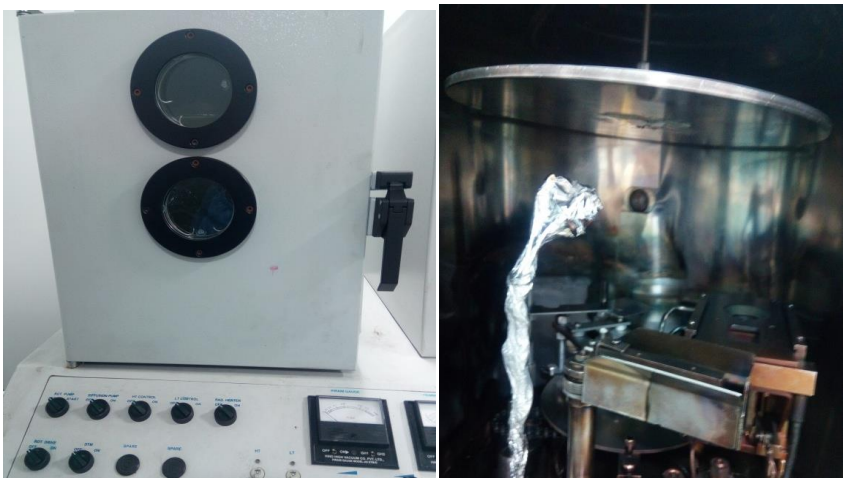

Fig. 4.11. a) Photograph of BC300 High Hind Vacuum box coater (thermal evaporator), b) inside picture of BC 300 HHV box coater [courtesy-microfabrication lab facility, Tezpur University].

PANi-Ta_2O_5-CSA nanocomposite was obtained as a fine dispersion by adding it in powdered form in NMP (N-methylpyrolidine) in 10wt% and stirred it on a magnetic stirrer for 4 hours.

The nanocomposite was then deposited on the PMMA layer using spin-coating technique at 1000 rpm for 80 seconds. The deposited layer was then dried in an oven at 50^0C for 1 hour. The thickness of the semiconductor layer was measured as 500 nm. Gold electrodes were defined as top source and drain contacts each with thickness 100±5 nm. The gold contacts were thermal evaporated with a hard mask in a physical thermal vacuum coating system (Fig.4.11- BC-300, Hind High Vacuum) maintaining the pressure at 2×10^{-5} Torr.

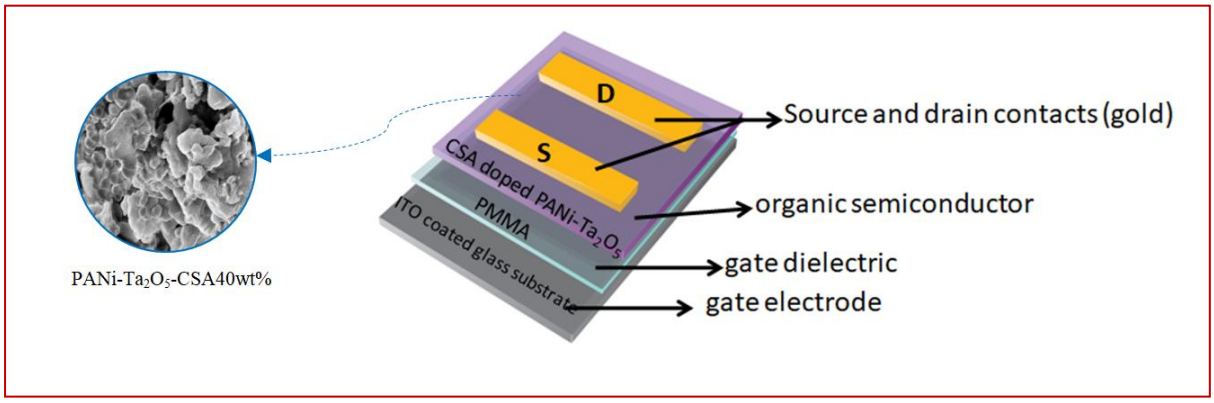

Fig.4.12. Schematic of the PANi-Ta_2O_5-CSA40% based OFET device with channel length 1 mm and channel width 1 cm [264].

The schematic of the PANi-Ta_2O_5-CSA40% based OFET with channel length (L) 1 mm and channel width (W) 1 cm was shown in Fig. 4.12. The dimensions of the studied OFET device fabricated are presented in table 4.1.

Table- 4.1

(Dimensions of the PANi-Ta_2O_5-CSA40% OFET device)

Thickness of (nm)				**Channel length (L)**	**Channel Width (W)**	**Capacitance per unit area (C_i) of PMMA**
Source contact	**Drain contact**	**Organic semiconductor layer**	**Gate dielectric**			
100±5	100±5	500	900	1 mm	1 cm	6.195×10^{-9} F/cm^2

The photograph of the fabricated PANi-Ta_2O_5-CSA based OFET device with ITO coated glass substrate (middle) is shown in Fig. 4.13. The two OFET devices on left and right side of the photograph were fabricated on glass substrate for testing purpose with SiO_2 as the gate dielectric and, aluminium source, drain and gate electrodes.

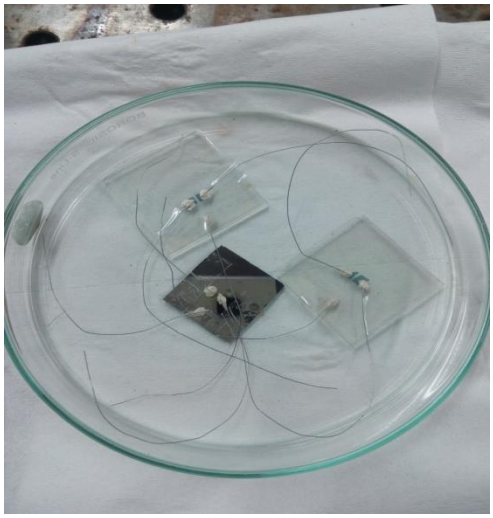

Fig.4.13. Photograph of the fabricated PANi-Ta_2O_5-CSA40% based OFET device (middle) with channel length 1 mm and channel width 1 cm.

4.4 Results and discussion

4.4.1. Electrical characterization

The electrical characterization of the OFET device was done using Keithly 2450 Sourcemeter and Keithly 2100 61/2-digit USB multimeter. All measurements were performed under ambient condition at 25^0C room temperature and 55% relative humidity. To measure the electrical characteristics, we studied the output characteristics and transfer characteristics of the CSA doped PANi-Ta_2O_5 based OFET device. For obtaining the output characteristics, the gate was biased with a constant voltage (V_{GS}) and a voltage was applied between the drain and the source (V_{DS}), with the source being grounded. V_{DS} was swept through 0 V to -50 V, while the corresponding value of I_{DS} was recorded. For each output plot, V_{GS} was kept fixed at 0 V though -50 V in steps of -10 V.

The output characteristics of the OFET are shown in Fig. 4.14. It is evident from here that, the conductance values are high initially at low V_{DS}, but decreases with increase in V_{DS}, indicating a good ohmic contact between the PANi-Ta_2O_5-CSA semiconducting layer and the source and drain electrodes. The magnitude of the drain-to-source current, I_{DS} is smaller and it depicts a quadratic dependence on V_{GS} in saturation, which has resulted from the long channel effect.

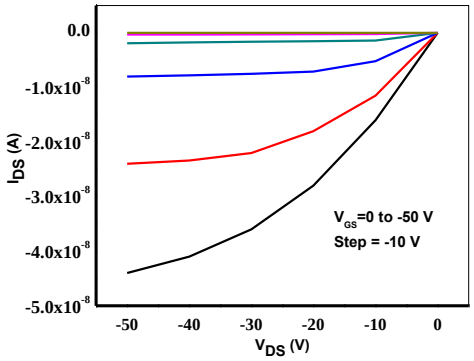

Fig. 4.14. Output characteristics of CSA doped PANi-Ta_2O_5 based OFET [264].

Fig. 4.15 shows the electrical connections made for obtaining the transfer plots of the OFET device. V_{DS} is kept fixed at -50 V. A voltage was applied between the gate and the source (V_{GS}), with the source being grounded. V_{GS} was swept through 0 V to -50 V, while the corresponding values of I_{DS} were recorded.

The transfer characteristics were obtained by plotting I_{DS} on a log scale as a function of V_{GS} for a V_{DS} of -50 V as shown in Fig. 4.15. The device exhibits a typical p-type characteristic. For negative V_{GS}, the device operates in accumulation mode with hole accumulation in the channel. When V_{GS} is positive, the semiconductor/dielectric interface becomes depleted of charge carriers and the device turns to depletion mode.

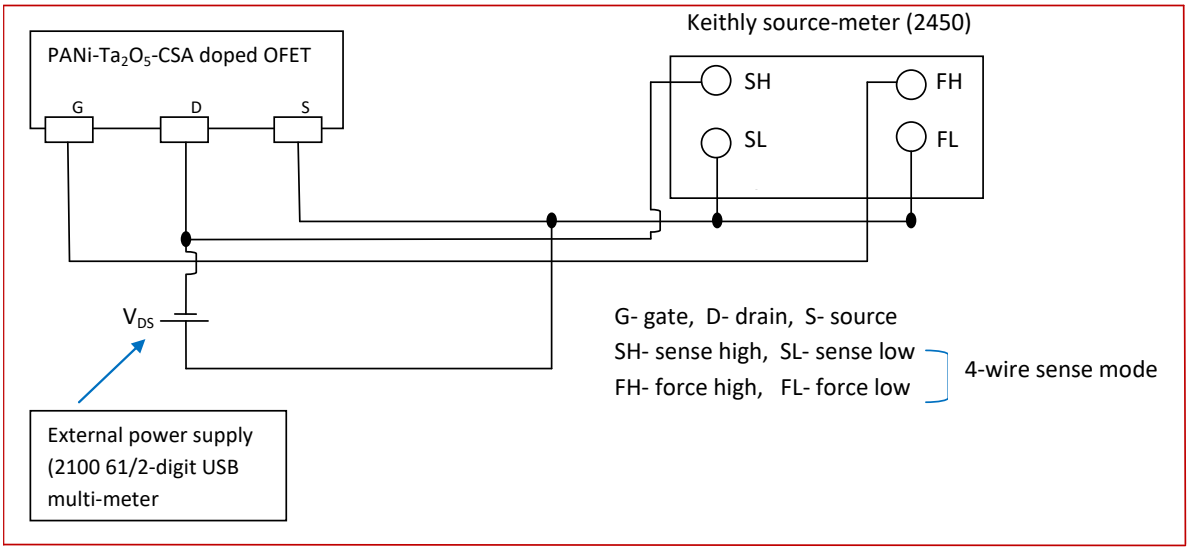

Fig. 4.15. Schematic of electrical connections of the PANi-Ta_2O_5-CSA based OFET for obtaining I_{DS} vs V_{GS} plots, keeping V_{DS} fixed.

The performance of the OFET is determined by the key parameters like the field-effect mobility (μ), the saturation current (Ion), the ON/OFF current ratio (I_{ON}/I_{OFF}), threshold voltage (V_{TH}) and sub threshold swing (SS). These parameters can be calculated from the transfer curves of the device as elaborated below.

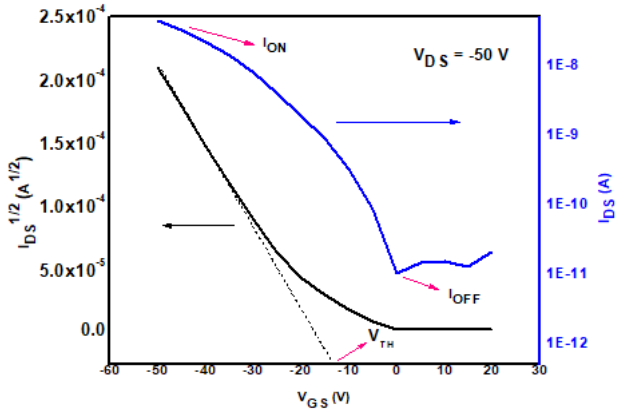

Fig. 4.16. Drain-source current ($|I_{DS}|$) plotted on log scale and square root of I_{DS}, ($|I_{DS}|^{1/2}$) as a function V_{GS} of CSA doped PANi-Ta_2O_5 based OFET, with μ= 0.12 cm^2/V-s, V_{TH} = -12.89 V and I_{ON}/I_{OFF} ~ 10^3 [264].

The field-effect mobility, μ was estimated from the transfer curve (Fig. 4.16) in the saturated regime and solving equation 4.4 (rewritten as equation 4.6).

$$I_{DS,SAT} = \frac{W}{L}\mu C_i \frac{1}{2}(V_G - V_{TH})^2 \qquad (4.6), \quad V_{DS} > (V_{GS}\text{-}V_{TH})$$

Here, W and L are the channel width and length and Ci is the capacitance of the gate dielectric per unit area. We have the following expression for carrier mobility at saturation. The validity of equation 4.6 is based on several assumptions like constant mobility and the equality in the density of the free carriers and dopants [272]. Equation 4.6 can be rewritten as follows.

$$\sqrt{I_{DS,SAT}} = \sqrt{\frac{W\mu C_i}{2L}}V_{GS} - \sqrt{\frac{W\mu C_i}{2L}}V_{TH} = a.V_{GS} - b \qquad (4.7)$$

Here, the values of μ and V_{TH} can be graphically extracted from the linear fit to equation 4.7 and from the square root of I_{DS} versus V_{GS} plot, where a and b are the slope and the x-axis intercept.

$$\mu_{sat} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2 \qquad (4.8)$$

or, from equation 4.7 we have

$$\mu_{SAT} = \frac{2L}{WC_i}a^2 \qquad (4.9)$$

$$V_{TH} = \frac{b}{a} \qquad (4.10)$$

The channel, L and the channel, W are 1 mm and 1 cm respectively and capacitance of PMMA per unit area, $C_i=6.195 \times 10^{-9}$ F/cm^2. The saturated-regime carrier mobility, μ near 0.12 cm^2/V-s and threshold voltage, V_{TH} near -12.89 V were obtained using the above parameters for the CSA doped PANi-Ta_2O_5 based OFET device.

Equation 4.6 depicts the dependence of drain current, I_{DS} and the gate voltage, V_{GS} in the saturation region. The device transits to saturation mode when the conducting channel gets "pinched off" at the drain end. This pinch-off is exerted by the increasing drain voltage, V_{DS}. If V_{DS} is further increased, the pinch-off point moves closer to the source. This reduces the channel region and the drain current gets smaller. This phenomenon is prominent in case of short-channel devices (short-channel effect).

Current on/off ratio (I_{ON}/I_{OFF}) can be calculated from the transfer curve (I_{DS} versus V_{GS} plot). It directly reflects the switching capability of the device. A high value of I_{ON}/I_{OFF} is desirable as it indicates a larger load drive capacity, better stability and less interference [269].

Current on/off ratio can be calculated from Fig. 4.13 by taking I_{ON} as I_{DS} at maximum values of V_{DS} and V_{GS} and I_{OFF} is the minimum of I_{DS} at maximum value of V_{DS}.The current on/off ratio was found near 10^3 when V_{GS} changes from -20V to 20 V. V_{TH} and I_{ON}/I_{OFF} are indicated in Fig. 4.16.

The device turns to on state when the gate voltage exceeds V_{TH} and a drain current is formed. Even at a lower gate voltage, a small current (I_{OFF}) exists due to diffusion of charge carriers due to their thermal energy. This area of operation is called subthreshold regime and it is quantitatively represented by subthreshold swing, SS. SS indicates the speed with which the device can be switched from off state to on state (i.e. the increase in I_{DS} with V_{GS}), with low values qualify for a better device [269]. The value of SS should be as low as possible as it indicates that a small value of ∂VGS is needed to turn on the device which is decisive for low power applications [256].

The relatively high charge carrier mobility of the CSA doped PANi-Ta_2O_5 device might have resulted from the decrease in source and drain contact resistance due to the long conducting channel causing weaker influence of the channel resistance [273]. High carrier mobility results into high conductivity which further facilitates charge transport in the active layer. This can contribute towards improved gas sensing feature of the semiconductor layer [274].

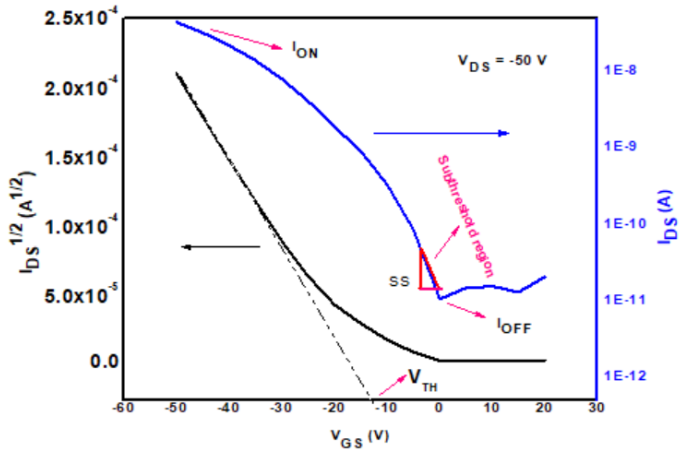

Fig. 4.17. Transfer curve of CSA doped PANi-Ta_2O_5 based OFET reproduced showing I_{ON}, I_{OFF}, V_{TH} and SS.

The subthreshold slope is the gate voltage necessary to change the drain current by one decade. The sub-threshold swing, SS is the inverse of subthreshold slope (Fig. 4.17) and was obtained from logarithmic plot of I_{DS} versus V_{GS} plot (equation 4.11) with a value of 9.3 V/dec.

$$SS = \left(\frac{\partial \log I_{DS}}{\partial V_{GS}} \right)^{-1} \qquad (4.11)$$

In general, OFETs exhibit a relatively large value of SS due to the localized trapping of holes near the HOMO level or that of electrons near LUMO level of the OSC. This may be also the reason for high threshold voltage. This is a common phenomenon observed in OFETS.There may other contributing factors to large values of SS, which is a shortcoming of OFETs, such as low dielectric capacitance, high parasitic capacitances at semiconductor/dielectric interface and low breakdown voltage [256]. It has been shown that steep subthreshold region can be realized using high capacitance gate dielectric [275].

The subthreshold swing can be used to estimate maximum trap density at the semiconductor interface using the following equation [256].

$$N^{max}{}_{trap} = \left(\frac{q\, SS \log(e)}{k_B T} - 1 \right) \frac{C_i}{q} \qquad (4.12)$$

Here, q is the electronic charge, SS is the subthreshold swing, e is the Euler's number, Ci is the capacitance of the gate dielectric per unit area, k_B is the Boltzmann's constant and T is the absolute temperature. Using the above equation, the maximum trap density of the studied OFET was found as 3.87×10^{10} cm^{-2}.

The CSA doped PANi-Ta_2O_5 based OFET exhibited a relatively high carrier mobility of 0.12 cm^2/V-s and a current ON/OFF ratio ~10^3. The relatively good performance was mainly attributed to the improved crystalline nature of the CSA doped PANi nanocomposite and the synergy between the semiconductor and the dielectric leading to a relatively low trap density at the dielectric interface.

As evident from the XRD results, the PANi-Ta_2O_5-CSA layer is polycrystalline in nature. The crystallinity of the nanocomposite became high with the addition of Ta_2O_5. Charge carriers are more mobile in crystalline regions in the polymer matrix due to the formation of highly ordered and stronger π-π stacking [276]. The values of carrier mobility in crystals are much higher than in the amorphous counterpart. There have been experimental findings

which establish that the improved molecular ordering achieved by solvent mixing or solution treatment before layer deposition can significantly enhance the carrier mobility [277]. Electrical characteristics of the CSA doped PANi-Ta_2O_5 based OFET are summarised in table 4.2.

The crystal size of pure PANi was calculated as 6.3 nm, whereas the crystal size of PANi-Ta_2O_5 increased to 12.49 nm. Carrier mobility improves as the crystal grain size increases with reduction in grain boundaries (i.e. no. of grains per unit area). Grain boundaries cause scattering of carriers causing lower mobilities [265].

Table- 4.2

(Summary of electrical properties of CSA doped PANi-Ta_2O_5 OFET)

Charge Carrier Mobility (μ)	**Threshold Voltage (V_{TH})**	**Current ON/OFF ratio (I_{ON}/I_{OFF})**	**Subthreshold swing (SS)**	**Maximun trap density at the semiconductor/dielectric interface (N^{max}_{trap})**
0.12 $cm^2/V\text{-}s$	-12.89 V	~10^3	9.3 V/dec	3.87 × 10^{10} cm^{-2}

The electronic property of the OFET can be influenced by several factors such as the morphology of the semiconductor and the dielectric, and the nature of the semiconductor/dielectric interface. Atomic force microscopy (AFM- Model No. NTEGRA Vita from NT-MDT) study was performed to get insights on the morphological properties and roughness features of the sensor device.

Fig. 4.18 shows the topographic image of the area between the source and drain contact areas of PANi-Ta_2O_5-CSA layer deposited on the PMMA dielectric layer. The AFM image reveals a well defined morphology of the PANi nanocomposite with granular microstructure bearing a root mean square (RMS) roughness of 0.764 nm.

The AFM results indicate a relatively smooth surface of the semiconductor layer being deposited over the dielectric layer. A smooth surface facilitates higher crystallinity with larger grains and can enhance gas adsorption process.

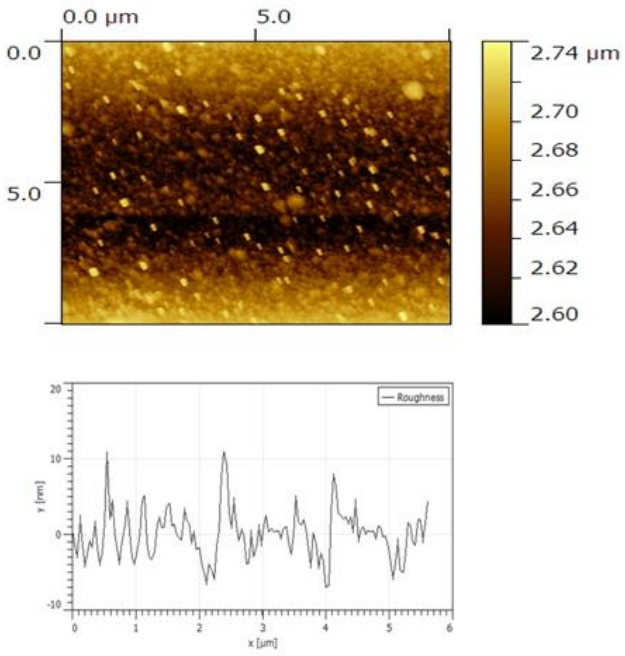

Fig. 4.18. AFM surface morphology of the CSA-PANi-Ta_2O_5 layer deposited on the PMMA layer with rms 0.764 nm [264].

It can be stated that the PMMA structure beneath the semiconductor layer might have favored in low density in grain boundaries and hence larger crystalline domain, and also on the formation of smooth semiconductor/dielectric interface. This has consequently led to improved carrier mobility. More research is needed to further correlate the OSC crystal grain size and the field-effect mobility taking into consideration of various factors like the OSC and the dielectric deposition process, rate of deposition and deposition temperature.

The incorporation of the polymeric gate dielectric played an important role towards the performance of the device. The solubility of PMMA rendered a good synergy between the former and the organic semiconductor and, helped in a favorable growth of the active layer [278]. This facilitates an improved interface leading to low leakage current (~10^{-11} A) and moderately high current on/off ratio [259]. Also, PMMA being hydrophobic in nature hinders the migration of contaminants into semiconductor-dielectric interface, thus reducing the no. of charge trapping sites [279].

4.4.2 Study of gas sensing characteristics

4.4.2.1 Experimental

The gas sensing properties of the CSA doped PANi-Ta_2O_5 OFET device were investigated towards various concentrations of NO_2 gas using the home-made gas sensing setup shown in Fig. 4.18, which was used earlier for the chemiresistive sensor. The NO_2 gas (1000 ppm calibration gas mixture: nitrogen dioxide plus balance nitrogen gas) was purchased from Spancan N Equipment, Salt Lake, Kolkata - 700064.

The sensor performance measurement of the PANi-Ta_2O_5-CSA based OFET device was carried out under ambient condition at 25^0C room temperature and 55% relative humidity using the home-built sensing unit (Fig. 4.19) connected to a Keithly 2450 Sourcemeter for current-voltage characterization. The OFET sensor was housed inside the glass chamber of 200 ml capacity of the gas sensing apparatus. NO_2 gas was diluted in nitogen carrier gas and injected at different concentrations, ranging from 10 ppm to 80 ppm in different periods of time. The change in drain current (I_{DS}) was carefully observed during each test and recorded. The gas flow rates were controlled using mass flow controllers (MFC). After each test of exposure, NO_2 gas was purged from the gas sensing chamber and the OFET sample was settled in the ambience of N_2 (200ml/min.) for 20 minutes.

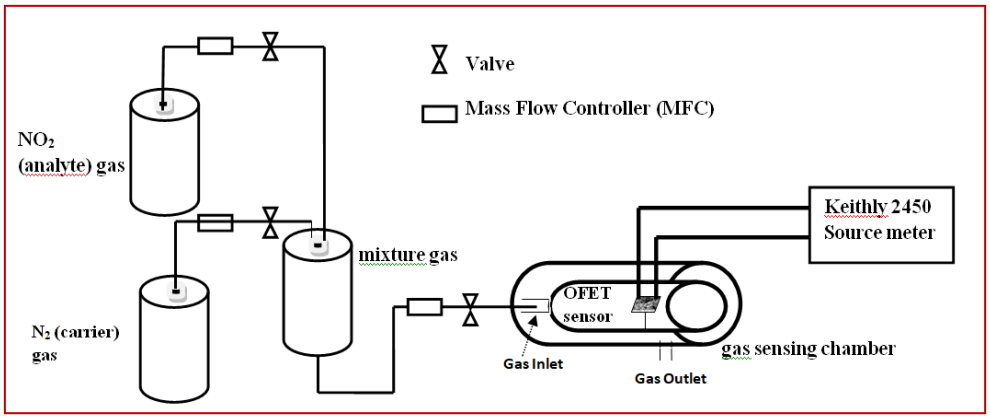

Fig.4.19. In-house gas sensing setup for examining NO_2 gas sensing properties of PANi-Ta_2O_5-CSA based OFET device [264].

For measuring the output characteristics for each concentration of NO_2 (0, 10, 20, 40, 60 and 80 ppm), the following voltage setting was made. The gate was biased at a fixed voltage (V_{GS} = -50 V). The source was grounded and the drain-to-source voltage, V_{DS} was swept through 0

V to -50 V, and the corresponding value of drain current, I_{DS} was recorded. The output plots of the device obtained without NO_2 exposure and then under subsequent exposure of different concentrations of NO_2 are shown in Fig.4.20.

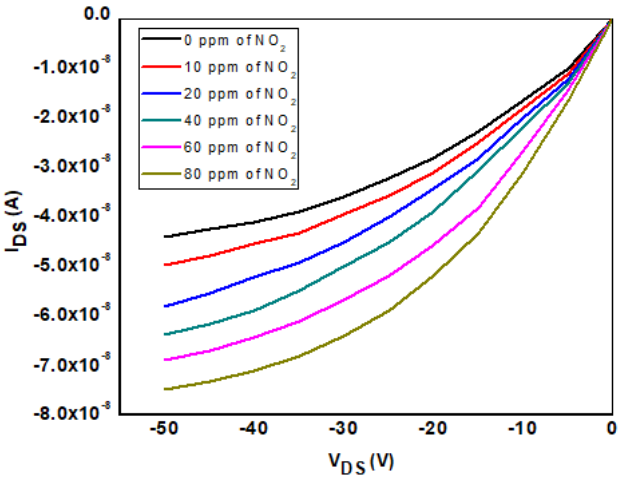

Fig. 4.20. Output curves of PANi-Ta_2O_5-CSA based OFET to various concentrations of NO_2 at V_{GS}=-50 V.

The percentage change in I_{ON} towards different NO_2 concentrations is shown in Fig. 4.21. The saturation current, I_{ON} showed significant change when exposed to different NO_2 concentrations. With 10 ppm, the change in the saturation drain current was 13%, whereas there has been around 70% change with 80 ppm gas concentration. Here, I_{NO2} and I_{N2} are the ON currents under the exposure of a certain conecentration of NO_2 and without the NO_2 gas respectively.

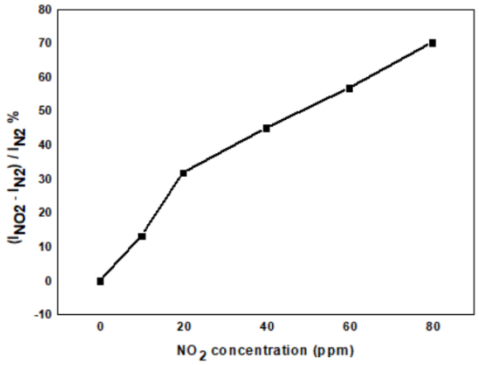

Fig. 4.21. Percentage variation of I_{ON} of PANi-Ta_2O_5-CSA based OFET to various concentrations of NO_2 at V_{GS}=V_{DS}=-50 V.

For obtaining the typical transfer plots under various concentrations of NO_2, each measurement was carried out at V_{DS} = -50 V, while V_{GS} was swept from -50 V to +20 V. The corresponding values of I_{DS} were recorded for each test accordingly and plotted as shown in Fig. 4.22. As revealed by the transfer plots, there has been gradual increase in drain current with increase in NO_2 concentration. It was also observed that both the threshold voltage, V_{TH} and carrier mobility significantly changed with increase in NO_2 gas concentration.

V_{TH} is related to the charge trapping at the dielectric/OSC interface. The larger no. of hole carriers captured at the interface, the higher negative gate voltage is needed to turn on the OFET and vice-versa. With NO_2 exposure, more hole carriers are generated in the channel, thus filling the traps to a great extent. The rest of the carriers then contribute to the current flow in the channel. This results in decrease in charge trap density in the interface, enhancement of carrier mobility (high carrier concentration leads to high carrier mobility) and positive shift in the threshold voltage [16]. This is observed in the Fig. 4.22.

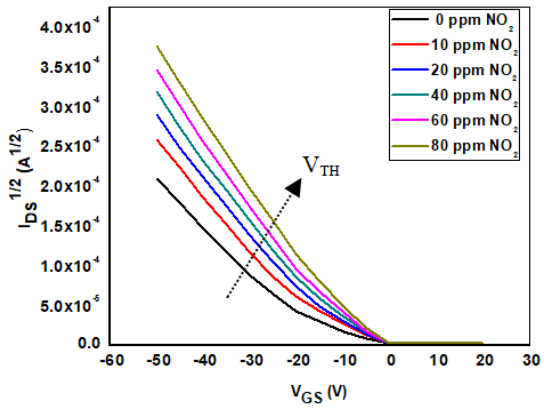

Fig. 4.22. Transfer curves of PANi-Ta_2O_5-CSA based OFET to various concentrations of NO_2 at V_{DS}=-50 V.

The change in threshold voltage (V_{TH}) and carrier mobility (μ) with different exposure to NO_2 is illustrated in Fig. 4.23. It can be seen that there has been positive shift of V_{TH} with the increase in the gas concentration and the rate of increase of carrier mobility was found higher.

NO_2 with strong electron affinity absorbs electron while interacting with the CSA-PANi-Ta_2O_5 layer and thus more hole carriers are generated. Theerfore, carrier concentration of the

device increases when exposed to NO_2. The first batch of injected carriers invades the traps under the transport energy level and then adds to the flow of current. The carrier concentration (n) determines the charge carrier mobility (μ) by the power law $\mu(n) \alpha n^{\delta}$. This means higher the carrier concentration is the greater is the carrier mobility [18].

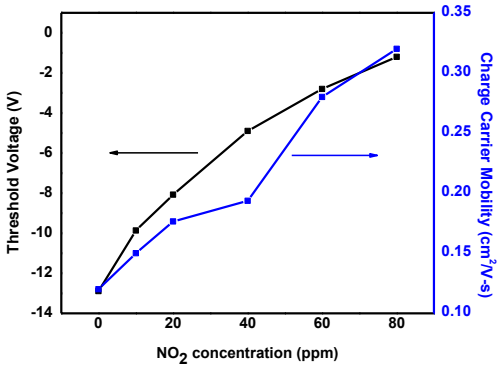

Fig. 4.23. Change in threshold voltage and carrier mobility at different concentrations of NO_2.

The real-time drain current (I_{DS}) response to NO_2 is shown in Fig.4.24. Both V_{DS} and V_{GS} were set at -50 V. The sensor response (S) of the OFET was evaluated by measuring the relative change in the drain current when exposed to a particular concentration of NO_2, defined by $S = \left|\frac{(I_{NO_2} - I_{N_2})}{I_{N_2}}\right| \times 100\%$ where I_{N2} and I_{NO2} are the drain currents in N_2 and in NO_2 respectively.

At the beginning of the experiment, the OFET device was rested in the gas chamber in N_2 atmosphere for 5 minutes. Once the device showed a stable value of I_{DS}, NO_2 was injected at a particular concentration. Three cycles of gas exposure were performed with 10 ppm, 30 ppm and 50 ppm of NO_2 gas. Each cycle lasted around 3 minutes. For each cycle, NO_2 gas was flowed in till the drain current saturated at a maximum value. Then the gas was flowed out and the device was allowed to recover back to its original steady state. We obtained an estimate of response time and recovery time of the device for each exposure and the reproducibility of the successive cycles.

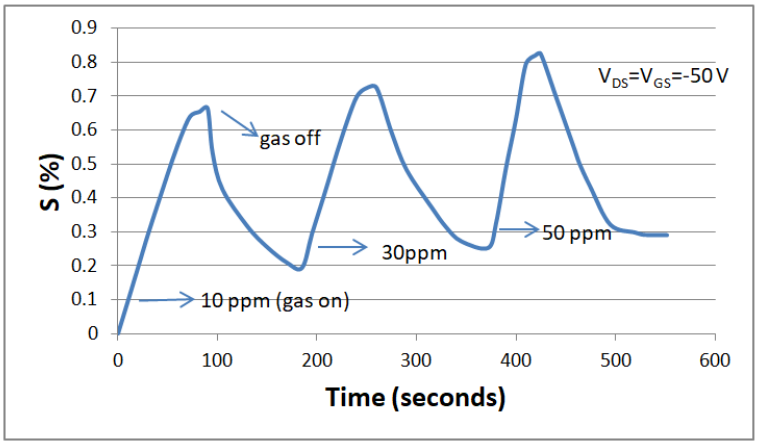

Fig. 4.24. Dynamic response of PANi-Ta_2O_5-CSA based OFET in three successive cycles to various concentrations of NO_2 at V_{DS}=V_{GS}=-50V.

It was revealed from Fig. 4.24, that the sensor response greatly increased with the increase in NO_2 concentration. With 50 ppm, the device showed a significant response of about 82.5%. The response time revealed a declining trend, while the recovery time took longer with increase in the gas concentration.

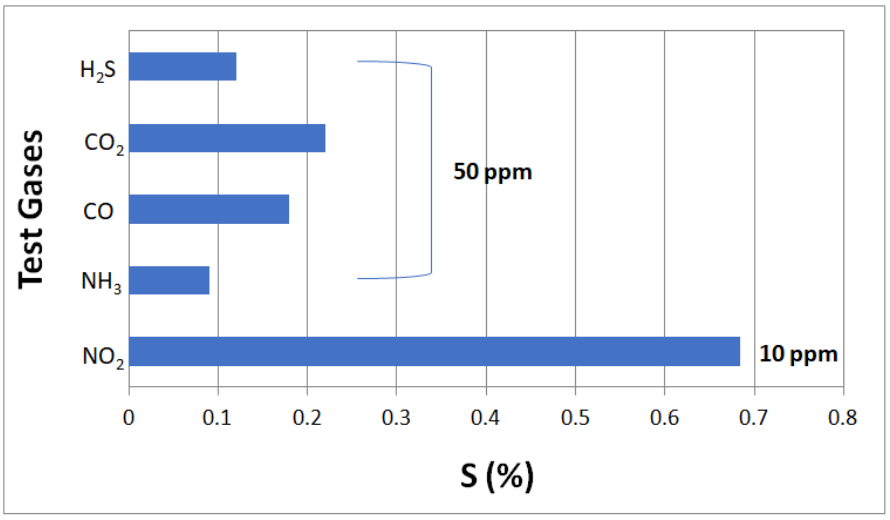

Fig. 4.25. Selectivity study of the PANi-Ta_2O_5-CSA based OFET.

The selectivity study was performed by measuring the sensitivity response, $S = \left|\frac{(I_{gas}-I_{N_2})}{I_{N_2}}\right| \times 100\%$ by exposing the PANi-Ta_2O_5-CSA doped OFET to 10 ppm of NO_2 and 50 ppm of a series of test gases, viz., NH_3, CO, CO_2 and H_2S. Here, I_{gas} and I_{N2} are the saturation drain

currents under the exposure of a certain conecentration of the analyte and without the analyte respectively. Each cycle of gas on and gas off lasted for about 3 minutes. As observed in Fig. 4.25, the device showed poor response to NH_3, CO, CO_2 and H_2S, while it showed significant response to NO_2 with sensitivity of 68.4%. Thus, it can be commented that the studied OFET sensor is highly selective to NO_2 and can be suitably used in practical applications for NO_2 gas sensing.The summary of the gas sensing results are produced in table 4.3.

Table- 4.3

(Summary of NO_2 gas sensing properties of PANi-Ta_2O_5-CSA based OFET)

NO_2 concentration (ppm)	**Sensor response, S (%)**	**Response time (seconds)**	**Recovery time (seconds)**
10	68.7 %	70	80
30	73.2%	65	97
50	82.5%	52	112

The gas sensing mechanism of the PANi-Ta_2O_5-CSA based sensing layer with the NO_2 analyte was described in detail in section 3.4.1 of chapter 3 of the chemeiresistive based sensor. The same mechanism applies to the OFET. The high sensor response of the OFET can be accounted for the strong electron withdrawal property of NO_2 and the 2D transfort route in the conducting channel further facilitated by the synergistic effect of the semiconductor layer and the underlying dielectric layer.

The high sensor response of the OFET device can further be accounted for the following factor. When the device comes in contact with NO_2, the deep traps in the grain boundaries are vastly filled resulting in diminishing the trap density and thereby reducing the trapping possibility of the injected hole carriers by the gate voltage. This is reflected in equation 4.11 for subthreshold swing (SS). The trap density N can be evaluated using equation 4.12.

As evident from equation 4.12, SS is proportional to trap density. The trap density at the OSC/dielectric interface without NO_2 gas was 6.04×10^{10} /cm^2 (for SS=9.3 V/dec). The trap density for different NO_2 concentrations and subthreshold swing were displayed in Fig. 4.26.

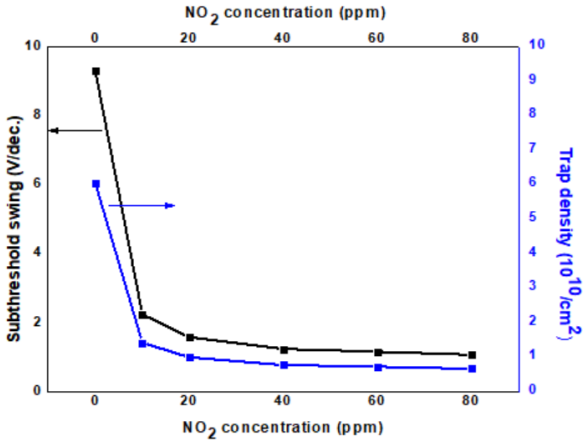

Fig. 4.26. Subthreshold swing and trap density change with NO_2 gas concentration of PANi-Ta_2O_5-CSA based OFET.

With 10 ppm NO_2 exposure, the trap density drastically reduced to 1.41×10^{10} /cm^2. As the gas concentration further increased, there has been decline in trap density but at a slower rate. This indicates that the generation of hole carriers saturated with further gas exposure and not very significant increase in drain current took place afterwards. The improvement of charge carrier mobility and positive shift of threshold voltage can also understood from the change in trap density with NO_2 exposure.

4.5. Chapter conclusions

This chapter illustrates the fabrication process and electrical characterization of CSA doped PANi-Ta_2O_5 based OFETs using PMMA as the gate dielectric. The surface morphology of the CSA doped PANi-Ta_2O_5 nanocomposite revealed highly aggregated spherical nanostructures. The AFM results showed a relatively smooth semiconductor layer with roughness (rms) 0.764 nm. The device achieved a relatively good charge carrier mobility of 0.12 cm^2/V-s and moderately high current on/off ratio lying in the order of 10^3. However, high operating voltage, large threshold voltage and subthreshold swing of the device were reported. The role of PMMA as the gate dielectric and improved crystallinity of the CSA doped PANi-Ta_2O_5 contributed significantly towards obtaining a relatively high charge carrier mobility of the device.

The fabrication process of the device found simple and cost–effective accompanied with easy material processibility. Thanks to the high solubility of the organic semiconductor and the polymer dielectric which undoubtedly enhanced the fine deposition of the respective layers.

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